REMARKS

This Amendment is filed in response to the Office Action dated March 10, 2003 (hereinafter the Office Action), which has a shortened statutory period set to expire June 10, 2003.

Applicants have amended Claims 1, 13, 15, 25, 26, 27, and 36 to clarify Applicants' invention.

Regarding the Examiner's remarks in paragraph 17 of the Office Action, Applicants agree that "a memory" is not an element of Claim 1. However, as correctly noted by the Examiner, Applicants have recited three memory models in Claim 1.

Regarding the rejection of Claim 1 under 35 U.S.C. 112, second paragraph, as being indefinite, Applicants have amended Claim 1 to recite in part "re-describing said simulation model of the memory". This amendment conforms to the Examiner's proposed modification noted in the Office Action. Therefore, based on this amendment, Applicants respectfully request reconsideration and withdrawal of the 112 rejection of Claim 1.

Regarding the rejection of Claims 1, 13, and 25 under 35 U.S.C. 103(a) as being unpatentable over Beausang in view of MPEP 2144.04(II)(A), Official Notice, and Cheng, Applicants have amended Claims 1, 13, and 25 to clarify Applicants' invention. Specifically, Claims 1, 13, and 25 now recite in part,

> if said memory is a read only memory (ROM), then proceeding directly to translating;
> if said memory is other than a ROM, then generating a simplified behavioral model of said memory by re-describing said simulation model of said memory with a predefined proper subset of said behavioral hardware description language;
> automatically translating said simulation model or said simplified behavioral model into said structural model of said memory, wherein said structural model comprises a plurality of ATPG memory primitives.

Applicants respectfully submit that the cited references fail to disclose or suggest these limitations.

Beausang teaches a computer implemented process and system for determining a set of sequential cells within an IC design that can be scan replaced. Col. 4, lines 57-59. Specifically, Beausang teaches selecting sequential cells for scan replacement that offer best testability contribution and not selecting sequential scan cells for scan replacement that do not offer much testability contribution and/or are part of most critical paths within the design. Col. 4, lines 59-67.

Applicants respectfully traverse any characterization of Beausang as teaching the memory models recited in Claims 1, 13, and 25. Specifically, Applicants submit that the selection process of Beausang does not teach anything regarding directly translating a simulation model into the structural model if the memory is a ROM and re-describing the simulation model into a simplified behavioral model if the memory is other than a ROM before translating that simplified behavioral model into the structural model.

Applicants now respond to the Office Action citation of Fig. 8 in Beausang. Element 605 in Fig. 8 includes an HDL description. Col. 14, lines 19-20. A generic compiler 615 transforms that HDL description into a technology independent netlist 620. Col. 14, lines 33-35. The technology independent netlist is then provided to a Test Ready (TR) compiler 625. Col. 14, lines 44-45. This TR compiler replaces the HDL memory cells with scannable memory cells (see Figs. 5A, 5B, 5C, and 5D for insertion of additional multiplexers and associated control lines) and inserts loopback connections (see Figs. 6A and 6B). Col. 14, lines 54-63.

The output of TR compiler 625, which is optimized using constraints 610, is a non-scannable technology specific netlist

630 (non-scannable because of its loopback connections). Col. 15, lines 1-3 and 11-14. Using a design rule checker 635, violated memory cells can be marked "unscanned". Col. 15, lines 35-37. This modified netlist can be provided to a scan insertion and routing logic block 645, which breaks the loopback connections in the scannable memory cells of the netlist and then constructs scan chains. Col. 15, lines 41-44 and 53-54. In this manner, a scannable mapped netlist 650 can be provided (in Beausang, at a system level) as input to an ATPG. Col. 16, lines 8-10.

Of importance, nothing described in reference to Fig. 8 or in other non-cited sections of Beausang teaches making a distinction between ROM and non-ROM and then re-describing the simulation model of the non-ROM memory.

Cheng fails to remedy the deficiency of Beausang. Specifically, Cheng teaches that most sequential circuit test generation approaches neglect circuit delays during test generation. Pages 406 (last line) and 407 (first line). However, of importance, Cheng teaches no distinction between ROM and non-ROM in generating the structural model of the memory.

Applicants respectfully submit that Judicial Notice cannot remedy the deficiencies of Beausang and Cheng. Specifically, Judicial Notice was taken only with respect to describing the simulation model in HDL.

Applicants also respectfully submit that MPEP 2144.04(II)(A) cannot remedy the deficiencies of Beausang and Cheng. MPEP 2144.04(II)(A) was cited with respect to Applicants' limitation of generating a simplified behavioral model. However, as noted previously, Beausang explicitly optimizes the output of TR compiler 625, i.e. non-scannable technology specific netlist 630, using constraints 610. Col. 15, lines 1-3 and 11-14. Therefore, contrary to the assertion

in the Office Action, it would not be obvious to modify Beausang by generating a simplified behavioral model of said memory (e.g. eliminating timing information or physical layout information). In fact, without such information, technology specific netlist 630 could not be optimized, which would teach away from Beausang. Additionally, MPEP 2144(II)(A) cannot address the recited distinction between ROM and non-ROM.

Based on the above remarks, Applicants request reconsideration and withdrawal of the rejection of Claims 1, 13, and 25.

Claims 2-12 depend from Claim 1, Claims 14-24 depend from Claim 13, and Claims 26-36 depend from Claim 25. Therefore, Claims 2-12, 14-24, and 26-36 are patentable for at least the reasons presented for Claims 1, 13, and 25.

Moreover, Claims 2, 14, and 26 recite in part "wherein said simplified behavioral model excludes timing information". As noted previously with respect to Claim 1, 13, and 25, Beausang explicitly optimizes the output of TR compiler 625, i.e. non-scannable technology specific netlist 630, using constraints 610. Col. 15, lines 1-3 and 11-14. Therefore, contrary to the assertion in the Office Action, it would not be obvious to modify Beausang by excluding timing information. In fact, without such information, technology specific netlist 630 could not be optimized, which would teach away from Beausang. Therefore, Applicants request further reconsideration and withdrawal of the rejection of Claims 2, 14, and 26.

Moreover, Claims 3, 15, and 27 recite in part "wherein said simplified behavioral model excludes physical layout information". As noted previously with respect to Claims 1, 13, and 25, Beausang explicitly optimizes the output of TR compiler 625, i.e. non-scannable technology specific netlist 630, using constraints 610. Col. 15, lines 1-3 and 11-14. Therefore,

contrary to the assertion in the Office Action, it would not be obvious to modify Beausang by excluding physical layout information. In fact, without such information, technology specific netlist 630 could not be optimized, which would teach away from Beausang. Therefore, Applicants request further reconsideration and withdrawal of the rejection of Claim 3.

Claims 5-8, 17-20, and 29-32 recite various limitations regarding the plurality of ATPG memory primitives. The Office Action cites Beausang at Col. 14, lines 39-43 as disclosing these limitations. Applicants respectfully traverse this characterization. This citation merely teaches that technology independent netlist 620 includes logical primitives and operators of the IC layout. A generalized statement regarding logical primitives does not disclose the primitives recited by Applicants. Therefore, Applicants request further reconsideration and withdrawal of the rejection of Claims 5-8, 17-20, and 29-32.

CONCLUSION & REQUEST FOR TELEPHONE INTERVIEW

Claims 1-36 are pending in the present Application. Applicants respectfully request allowance of these claims. If the Examiner next action is other than allowance, Applicants request the opportunity to speak with the Examiner in a telephone interview to clarify any remaining issues.

If there are any questions, please telephone the undersigned at 408-451-4907 to expedite prosecution of this case.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 5, 2003.

6/5/03 Robert A. Baumann
Date Signature